CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a clock tree comprising a coaxial clock line, the coaxial clock line comprising a substantially tubular outer conductor and an inner conductor, the substantially tubular outer conductor forming a substantially enclosed channel that extends in a direction, and wherein the inner conductor extends in the direction axially inside the substantially enclosed channel; and

a latch circuit having an input lead and an output lead, the input lead of the latch circuit being programmably capacitively coupleable to the inner conductor of the coaxial clock line.

2. The integrated circuit of Claim 1, wherein the input lead of the latch circuit is connected to a first conductive plate, wherein a second conductive plate is disposed at least in part in an opening in the substantially tubular outer conductor, wherein the input lead of the latch circuit is capacitively coupled to the inner conductor when the second conductive plate is floating, and wherein the input lead of the latch circuit is not capacitively coupled to the inner conductor when the second conductive plate is driven with a DC voltage.

3. The integrated circuit of Claim 2, wherein the DC voltage is ground potential.

4. The integrated circuit of Claim 2, wherein the first conductive plate has a planar surface disposed in a first plane, and wherein the second conductive plate has a planar surface disposed in a second plane, the first conductive plane being parallel to the second plane such that the first plane does not intersect the second plane.

5. The integrated circuit of Claim 2, wherein the second conductive plate is disposed between the inner conductor and the first conductive plate.

6. The integrated circuit of Claim 2, further comprising:

a memory cell having an output lead that is coupled to the second conductive plate.

7. The integrated circuit of Claim 1, wherein a signal having an edge is present on the inner conductor, and wherein the edge is coupled onto the input lead of the latch circuit thereby causing the latch circuit to switch from storing a first digital logic value to storing a second digital logic value.

8. The integrated circuit of Claim 1, wherein the substantially enclosed channel has a substantially rectangular cross-sectional shape.

9. The integrated circuit of Claim 1, further comprising:

a second latch circuit having an input lead and an output lead, the input lead of the second latch circuit being programmably capacitively coupleable to the inner conductor of the coaxial clock line.

10. An integrated circuit, comprising:

a clock tree comprising a coaxial clock line, the coaxial clock line comprising a substantially tubular outer conductor and an inner conductor, the substantially tubular outer conductor forming a substantially enclosed channel that extends in a direction, and wherein the inner conductor extends in the direction axially inside the substantially enclosed channel; and

a latch circuit having an input lead and an output lead, the input lead of the latch circuit being capacitively

coupled to the inner conductor of the coaxial clock line.

11. The integrated circuit of Claim 10, further comprising:

a clock conductor; and

a configuration memory cell that stores a bit of configuration data, wherein the latch circuit is enabled to drive a signal onto the clock conductor if the bit of configuration data has a first digital logic value, and wherein the latch circuit is disabled from driving a signal onto the clock conductor if the bit of configuration data has a second digital logic value.

12. The integrated circuit of Claim 11, wherein a first terminal of a field effect transistor is coupled to the output lead of the latch circuit, wherein a second terminal of the field effect transistor is coupled to the clock conductor, and wherein a third terminal of the field effect transistor is coupled to an output lead of the configuration memory cell.

13. A method, comprising:

distributing a clock signal via a clock tree across an integrated circuit to a plurality of latch circuits, each of the latch circuits having an input lead; and

loading configuration data into a plurality of configuration memory cells, wherein a bit of configuration data is stored in each configuration memory cell, the bit of configuration data stored in a configuration memory cell determining whether the input lead of an associated one of the latch circuits is capacitively coupled to the clock tree.

14. The method of Claim 13, wherein the input lead of each of the latch circuits is coupled to a conductive plate, the method further comprising:

providing a bias voltage on the input lead of each of the latch circuits.

15. A method, comprising:

distributing a clock signal via a clock tree across an integrated circuit to a plurality of latch circuits, each of the plurality of latch circuits having an input lead that is capacitively coupled to the clock tree, each of the plurality of latch circuits having an associated clock conductor; and

loading configuration data into a plurality of configuration memory cells, wherein a bit of configuration data is stored in each configuration memory cell, the bit of configuration data stored in a configuration memory cell determining whether an associated one of the latch circuits is enabled to drive a signal onto the clock conductor associated with the latch circuit.

16. The method of Claim 15, method further comprising:

providing a bias voltage on the input lead of each of the plurality of latch circuits.

17. An integrated circuit comprising:

a coaxial clock tree;

a clock conductor; and

means for capacitively coupling to the coaxial clock tree such that a clock signal present on the coaxial clock tree is capacitively coupled into the means and is supplied by the means onto the clock conductor if the means is configured in a first way, and wherein the clock signal present on the coaxial clock tree is not capacitively coupled into the means and is not supplied by the means onto the clock conductor if the means is configured in a second way.

18. The integrated circuit of Claim 17, further comprising:

a memory cell, wherein the means is configured in the first way when the memory cell stores a first digital logic value, and wherein the means is configured in a second way when the memory cell stores a second digital logic value.

19. The integrated circuit of Claim 18, wherein a second plate is disposed between the first plate and the coaxial clock line, the second plate being coupled to an output lead of the memory cell.

20. The integrated circuit of Claim 17, wherein the means comprises a first plate that is capacitively coupled to the coaxial clock line if the means is configured in the first way, wherein the means further comprises a latch circuit, the latch circuit having an input lead and an output lead, the input lead of the latch circuit being coupled to the first plate, the output lead of the latch circuit being coupled to the clock conductor.